What is claimed is:

1. A method of evaluating a layer matching deviation based on CAD information, the method comprising:

storing design CAD data of a semiconductor device formed on a semiconductor wafer; and

reading the design CAD data of a pattern of the semiconductor device and overlapping the design CAD data with an electron microscope image of the pattern formed on the semiconductor wafer on a display so as to evaluate acceptability of the formation of the pattern.

2. A method of evaluating a layer matching deviation based on CAD information, the method comprising:

storing design CAD data of a semiconductor device formed on a semiconductor wafer;

reading the design CAD data of a first pattern of the semiconductor device and overlapping the design CAD data with an electron microscope image of the first pattern formed on the semiconductor wafer on a display so as to evaluate acceptability of the formation of the pattern; and

further overlapping a design CAD image of a second pattern which is formed in a later step and related to the first pattern so as to evaluate acceptability of formation of the first pattern with regard to a relative relationship with the second pattern

3. An apparatus of evaluating a layer matching deviation based on CAD information, the apparatus comprising:

means for storing design CAD data;

means for displaying to overlap a scanning microscope image of a pattern of a semiconductor device formed on a wafer with a design CAD image read from the storing means on a display,

wherein acceptability of formation of the first pattern is evaluated by displaying to overlap a first pattern image of the semiconductor device formed on the wafer with the design CAD image of the first pattern, and the acceptability of the formation of the first pattern also is evaluated with regard to a relative relationship with a second pattern which is formed in a later step and related to the first pattern by displaying to overlap the second pattern with the overlapped images.

4. The apparatus of evaluating a layer matching deviation based on CAD information according to Claim 2, further comprising means for sampling a contour line segment from the microscope image, wherein the pattern image of the semiconductor device formed on the wafer is a pattern contour line segment sampled by the contour line segment sampling means.

5. The apparatus of evaluating a layer matching deviation based on CAD information according to Claim 3 having a navigation apparatus comprising means for providing a low magnification microscope image by controlling a stage based on position information, means for calculating a deviation amount by information of a CAD line segment and a matching processing on the low magnification microscope image in order to catch

a pattern image of a predetermined portion at a center of a field of vision by a microscope having high magnification.

6. The apparatus of evaluating a layer matching deviation based on CAD information according to Claim 4 having a navigation apparatus comprising means for providing a low magnification microscope image by controlling a stage based on position information, means for calculating a deviation amount by information of a CAD line segment and a matching processing on the low magnification microscope image in order to catch a pattern image of a predetermined portion at a center of a field of vision by a microscope having high magnification.